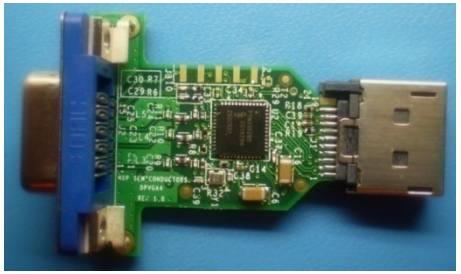
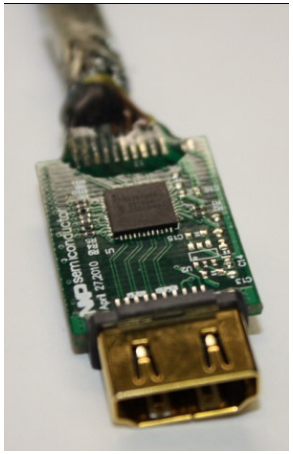




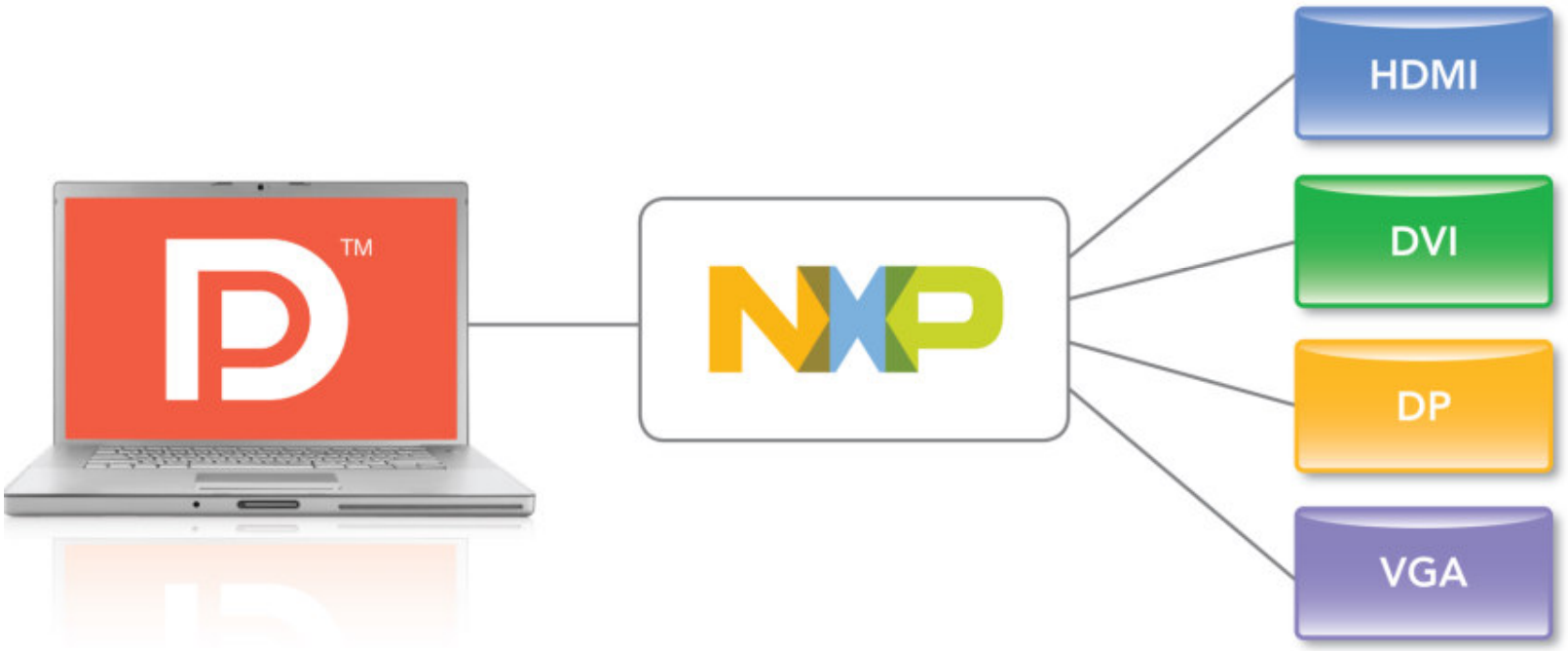
Display Port Adapters

PLIP Level II training in Shenzhen

David Li David.j.li@NXP.com
NXP Semiconductors

June, 2010

NXP enables DisplayPort



Contents

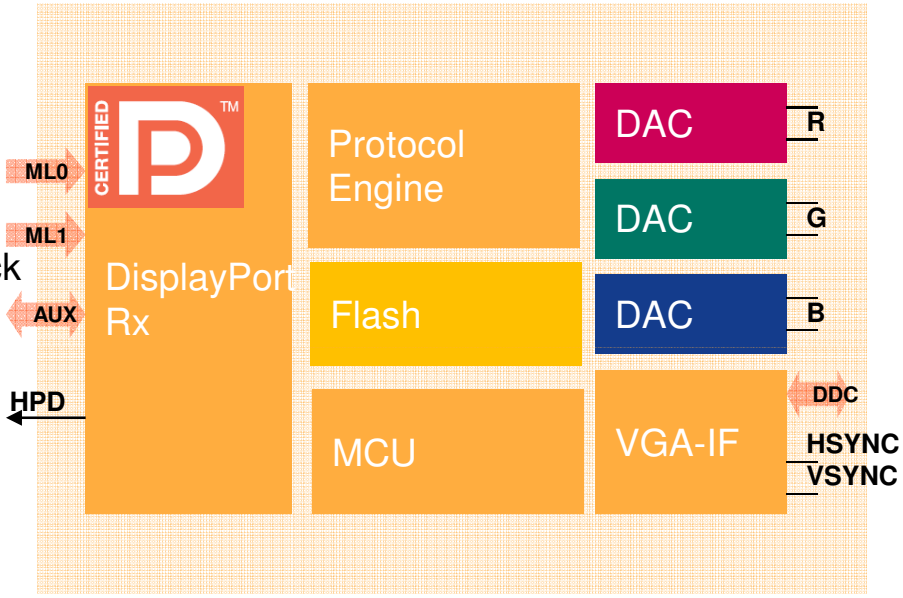
- NXP's DisplayPort-VGA Adapter PTN3392
  - Our Value Propositions
  - BOM Cost
  - DPVGA4 and DPVGA4M Reference Dongle Designs
  - Summary Test Results
- NXP's DisplayPort Roadmap
  - Next: PTN3372 is the same as PTN3392, and includes 5V regulator to achieve even lower system BOM
  - Low-Power DisplayPort-VGA Adapter PTN3352
    - NXP's DisplayPort-DVI and DisplayPort-HDMI solutions
- Appendices for PTN3392
  - Firmware Update via Host: Flash over AUX
  - Compliance, Interop, EMI, ESD Tests Results

NXP DisplayPort Adapter Products

Part Number	Status
PTN3360A, PTN3360B Enhanced DisplayPort-DVI/HDMI Level Shifters (Follow-up versions of PTN3300A, PTN3300B)	Production
PTN3361B Enhanced DisplayPort-DVI/HDMI Level Shifters w/ DDC buffer, feature optimized for dongle application	Production
PTN3380B Enhanced DisplayPort-DVI/HDMI Level Shifters w/ 5V voltage regulator, cost and feature optimized for dongle application	Production
PTN3381B Enhanced DisplayPort-DVI/HDMI Level Shifters w/ DDC buffer and 5V voltage regulator, cost and feature optimized for dongle application	Sampling Now
PTN3360D Enhanced DisplayPort-HDMI Level Shifter with Deep Color Support for HDMI on Motherboard	Production
PTN3392 2-lane DisplayPort-to-VGA Adaptor IC, cost and feature optimized for VGA dongle	Production
PTN3372 2-lane DisplayPort-to-VGA Adaptor IC, w/ 5V voltage regulator, cost and feature optimized for VGA dongle	Sampling Now

PTN3392 - DisplayPort to VGA Bridge

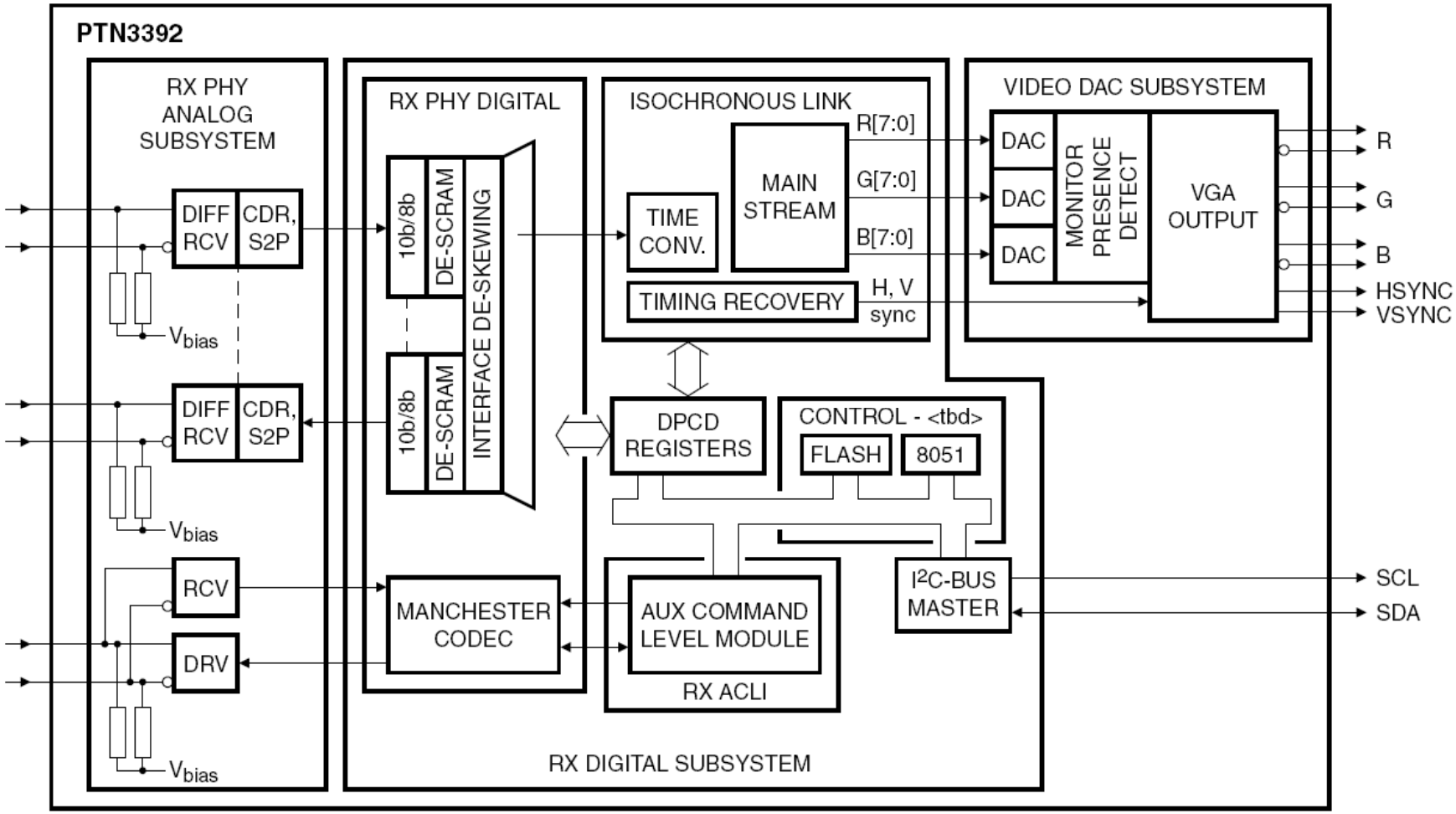
- DisplayPort receiver v1.1a
  - 1-lane / 2-lane 2.7Gb/s / 1.62Gb/s
  - AUX channel, HPD support
- Output
  - Analog RGB, HSYNC, VSYNC
  - Up to 240MHz, 8bits color
  - DDC
- Resolutions
  - WUXGA: 1920 x 1200, 60Hz, 193MHz clock
  - UXGA: 1600 x 1200, 60Hz, 162MHz clock
  - SXGA (CRT): 1280 x 1024, 80Hz, 135MHz clock
  - SXGA: 1280 x 1024, 60Hz, 108MHz clock
  - XGA: 1024 x 768, 60Hz, 65MHz clock
  - VGA: 640 x 480, 60Hz, 25MHz clock
- AUX channel to I²C DDC channel bridge
- Supports Flash over AUX field upgradability
- Use only power from DP connector 3.3V
- < 610mW Active @ 1920 x 1200; 150mW Standby; 500mW Init
- No support for HDCP and audio
- HVQFN48, 7x7mm, 0.5mm pitch
- ESD 7kV HBM



DP configuration	RBR: 1.62 Gbps	HBR: 2.70 Gbps
1 Lane	XGA, SDTV	SXGA, 1080i
2 Lanes	SXGA, 1080i	WUXGA

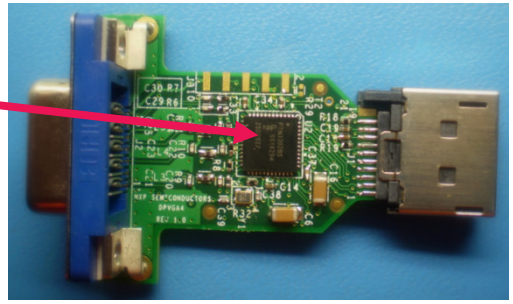
In Production

PTN3392 Block Diagram



NXP's DisplayPort-VGA Dongle

- PTN3392 has Embedded Flash
  - PTN3392 DisplayPort-VGA Adapter
  - 27 MHz crystal
  - 3.3V-to-5V regulator
  - No Need For
    - External flash
    - 3.3V-to-1.2V LDO
    - External ESD protection
  - PTN3372 integrates 3.3V-to-5V regulator



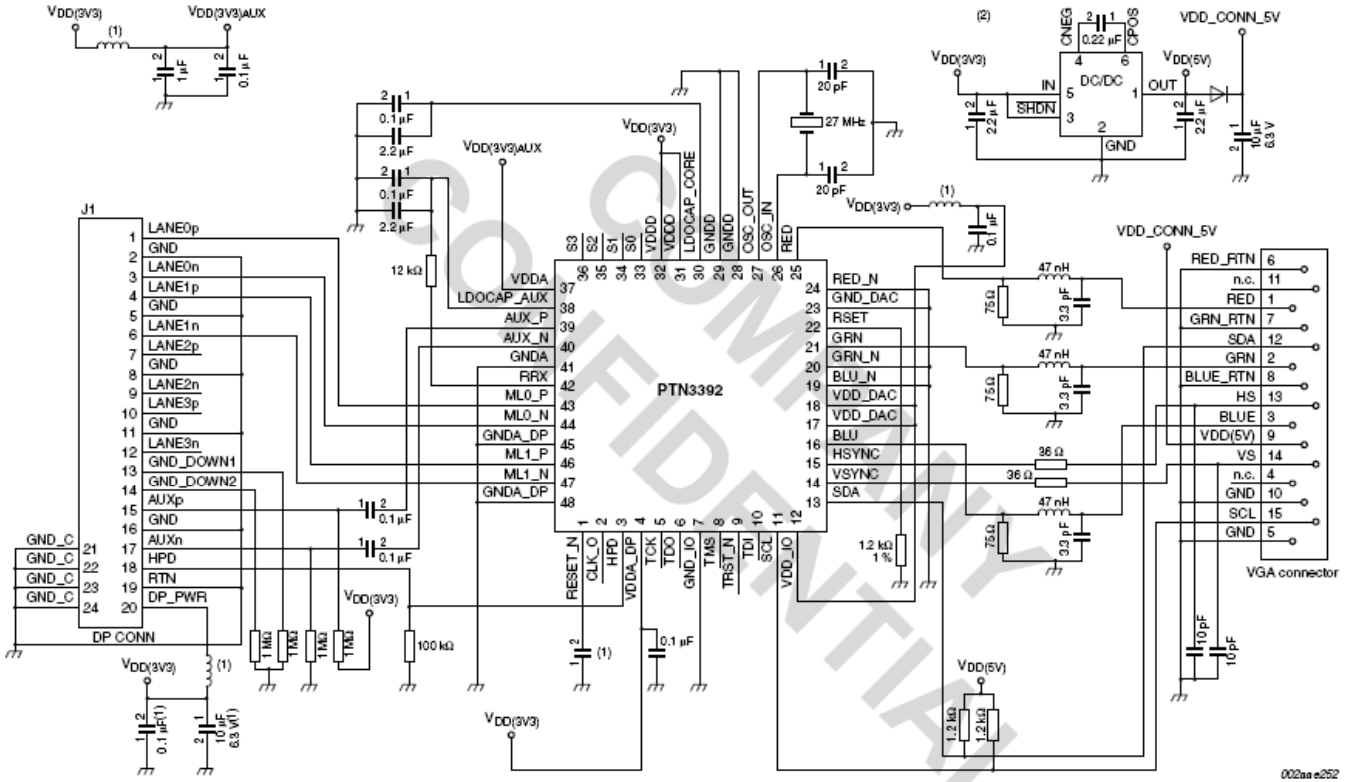
- Pros
  - Industry's lowest component count and BOM
  - Enable small-size dongle with smallest package and low BOM
  - Monitor detect by load sensing allows DP source; Support power saving upon monitor detachment
  - Flash programming over AUX CH, enabling future firmware driver download from the host
  - Interoperability

Good interoperability

  - MacBook Pro/ NVIDIA 9400M / 9600GT
  - Windows / Dell Latitude E5400 / Intel GMA4500
  - Windows / Dell Latitude E6500 / NVIDIA Quadro NVS160M
  - Windows / Dell Studio 1440 / NVIDIA GeForce 9400M
  - Windows / Lenovo THINKPAD W700 / NVIDIA Quadro FX2700
  - Windows / NVIDIA Zotac GeForce 9400GT GPU Card
  - Windows / ATI Radeon HD5750 GPU Card
  - Windows / HP ProBook 5310m / Intel GMA 4500

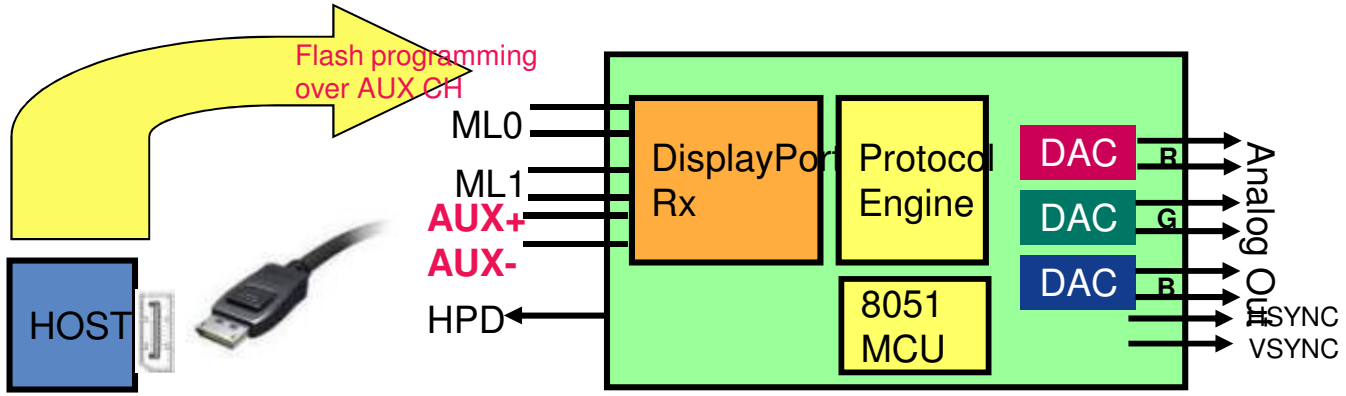
PTN3392 Bill of Materials

- Industry's Lowest System BOM
  - PTN3392
  - 27 MHz crystal
  - 3.3V-to-5V regulator
  - Filter for VGA
- No Need For
  - External flash
  - 3.3V-to-1.2V LDO



PTN3392 Firmware Update Via the Host AUX CH

- Interoperability issues due to …
  - "Holes" in DP specification and interoperability guidelines document
  - Differences in spec interpretation between DP TX and RX vendors
  - Workaround solutions
  - Insufficient regression testing of DP source driver updates
- Value Proposition of Flash Programming over AUX CH
  - Uses host computer to download firmware fix or upgrade to dongle
  - **Without additional hardware**
  - NXP will host a web site for dongle end users to download various dongle firmware versions
- Implementation depends on availability of SDK from GPU vendors allowing the feature
  - **NVIDIA / Windows** **NXP's implementation ready**
  - **AMD / Windows** **NXP's implementation ready**
  - **Intel / Windows** **NXP's implementation ready**

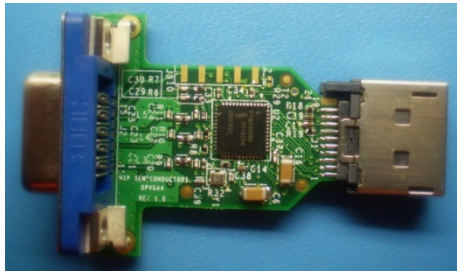


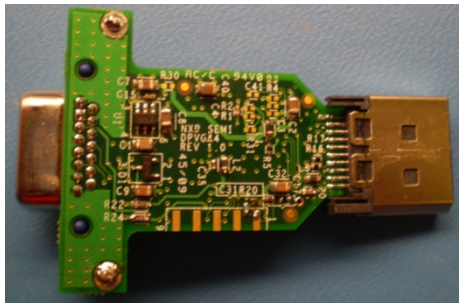
DPVGA4

NXP DP-VGA reference design dongle with PTN3392 and PTN3372

- Availability: NOW
- Reference Dongle Design
  - Uses PTN3392 or PTN3372 (stuff option)
  - Form factor close to a real dongle (but with still some debug capabilities)
  - Reflects best practices in schematics & layout
  - Reflects best-in-class BOM cost
  - Optimized for EMI
  - Optimized for VSIS performance
  - Purity of signals, reference planes
  - Final PTN3392 reference design schematic and BOM
  - Minimized size
  - Optimized component cost / quality
  - No external ESD protection needed for passing IEC ESD tests

- Contents
  - Full schematic and layout
  - Bill of Materials
  - Design and layout guidelines for optimal performance and EMC
- Purposes
  1. Customer reference design
  2. PTN3392 interop testing
  3. Trade show demos

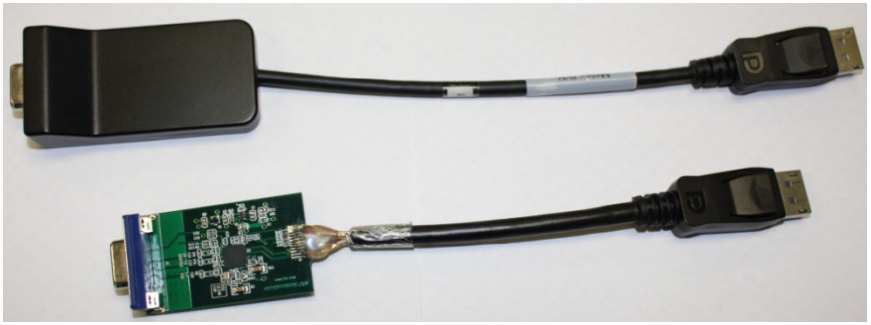




DPVGA4M

NXP DP-VGA reference design dongle with PTN3392 and PTN3372 Complete with plastic encasing

- Availability: NOW
- Reference Dongle Design
  - Uses PTN3392 or PTN3372 (stuff option)
  - Production-ready form factor
  - Reflects best practices in schematics & layout
  - Reflects best-in-class BOM cost
  - Optimized for EMI
  - Optimized for VSIS performance
  - Purity of signals, reference planes
  - Final PTN3392 reference design schematic and BOM
  - Minimized size
  - Optimized component cost / quality
  - No external ESD protection needed for passing IEC ESD tests
- Contents
  - Full schematic and layout
  - Bill of Materials
  - Design and layout guidelines for optimal performance and EMC



PTN3392 Test Status Summary

- DisplayPort v1.1a PHY-Layer Compliance Tests
  - Spec: VESA DisplayPort PHY CTS 1.1 or latest governing specification
  - Setup: Tektronix AWG Compliance Test Suite
  - Conditions: RBR & HBR, across supply voltage and temperature
  - Status: **ALL PASS**
- DisplayPort v1.1a Link-Layer Compliance Tests
  - Spec: VESA DisplayPort LLC CTS 1.1a or latest governing specification
  - Setup: Quantum Data DisplayPort Link-Layer Analyzer
  - Status: **ALL PASS**
- DisplayPort AUX CH Compliance Tests (Preliminary Results at Yokohama VESA Plugtest Dec 2009)
  - Status: **PASS**
- Inrush Current Tests
  - Status: **PASS**
- VSIS 1.2 Compliance Tests
  - Spec: VESA VSIS v1.r2
  - Setup: Tektronix VM6000 VSIS Compliance Test Suite
  - Conditions: 800 x 600, 60Hz, DMT, 40MHz ; 800 x 600, 85Hz, DMT, 56MHz; 1024 x 768, 75Hz, DMT, 81MHz ; 1600 x 1200, 65Hz, DMT, 175MHz
  - Status: **PASS**
  - DPVGA4 board - Final BOM optimization is in progress
- EMI Tests
  - Spec: CISPR22B
  - Setup: EMI chamber test
  - Status: **PASS** without metal shielding, but without the needed 3-6dB margin
  - Recommend use of metal tape around VGA connector or use of metal can to pass EMI tests with sufficient margin
- ESD Tests
  - Spec: IEC61000-4-2 8 kV contact discharge, 15 kV air discharge
  - Setup: Only applicable on over-molded version of dongle
  - Status: **PASS** without external ESD protection

PTN3392 Order Entry Options

PTN3392BS

- BS = HVQFN48 plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; 7x7x0.85 mm SOT619-1
- "Trust NXP" option – automatic firmware upgrades
- Backward compatible firmware
- Customer automatically gets latest firmware version

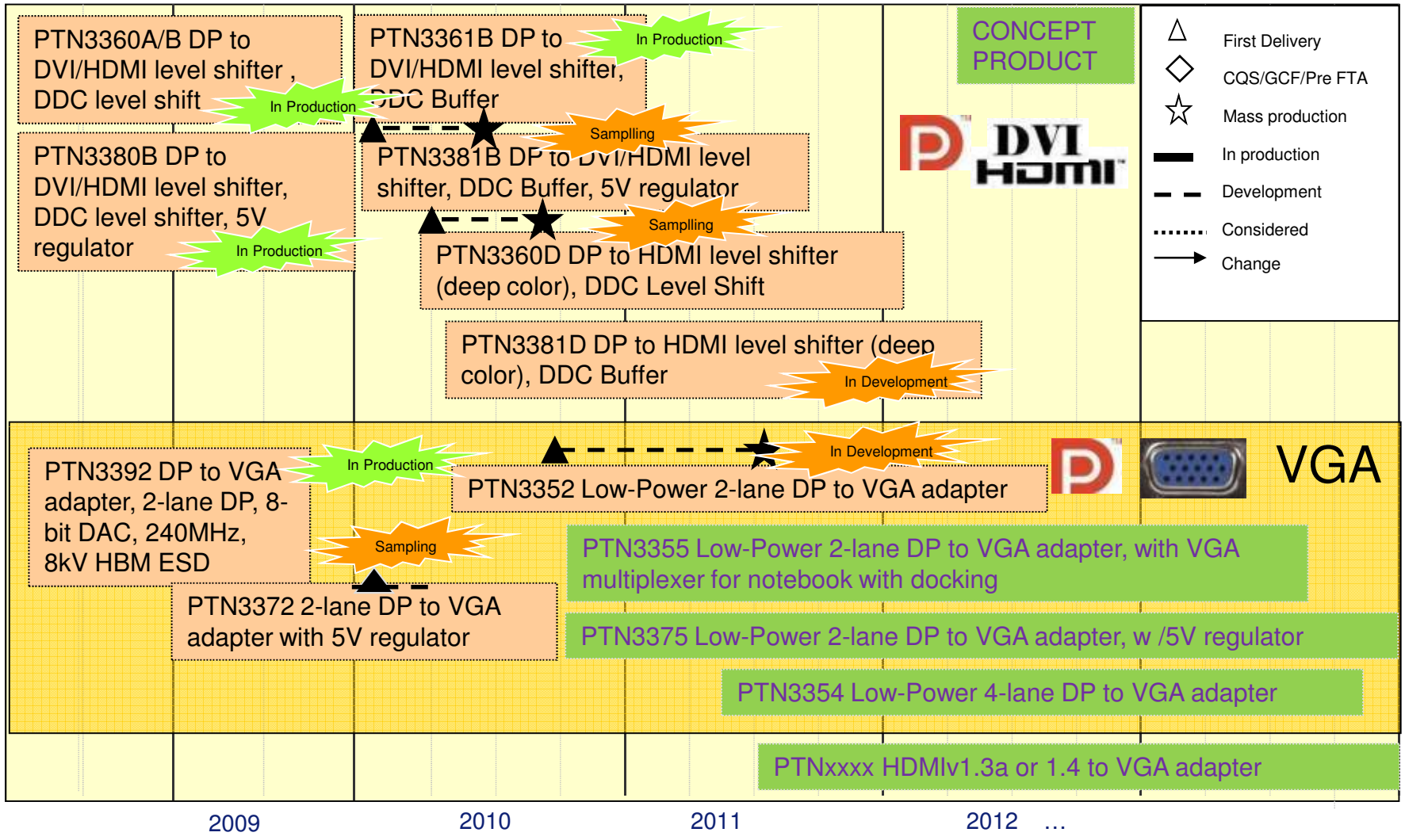
PTN3392BS/Fx

- BS = HVQFN48 plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; 7x7x0.85 mm SOT619-1
- Fx = Firmware identification option (Fx= 1,2,3, etc and indicates latest firmware version)
- Firmware version reflected on shipping box and reel but not on part symbol
- Firmware options will be identified by periodic Application Sheet updates, not by PCN
- Fx option must be selected at order entry
- Gives customer option of controlling firmware version

DisplayPort-VGA Adapter Roadmap

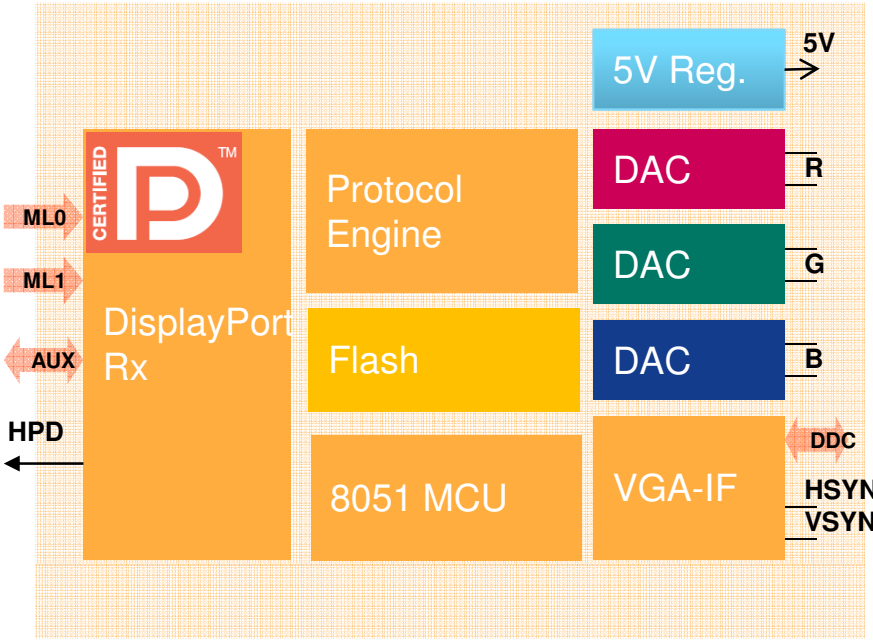
June 22, 2010

DisplayPort Adapter Roadmap Bridging to DVI/HDMI/VGA



PTN3372 – DisplayPort to VGA Bridge with 5V Regulator

- **DisplayPort receiver v1.1a**
  - 1-lane / 2-lane 2.7Gb/s / 1.62Gb/s
  - AUX channel, HPD support
- **Output**
  - Analog RGB, HSYNC, VSYNC
  - Up to 240MHz, 8bits color
  - DDC
- **Resolutions**
  - WUXGA: 1920 x 1200, 60Hz, 193MHz clock
  - UXGA: 1600 x 1200, 60Hz, 162MHz clock
  - SXGA (CRT): 1280 x 1024, 80Hz, 135MHz clock
  - SXGA: 1280 x 1024, 60Hz, 108MHz clock
  - XGA: 1024 x 768, 60Hz, 65MHz clock
  - VGA: 640 x 480, 60Hz, 25MHz clock
- Aux channel to I²C DDC channel bridge
- Supports Flash over AUX field upgradability
- 3.3V supply; 0 … 85 °C
- <700mW active; 150mW standby
- No support for HDCP or audio
- HVQFN48, 7x7mm, 0.5mm pitch
- ESD HBM 7kV
- PTN3372 = PTN3392 + Integrated 3.3V to 5V Voltage Reg
  - **Integrated solution for Low-cost DP-VGA Dongle**
  - **Lowest system BOM**
  - 3.3V to 5V voltage regulator supports 75mA load

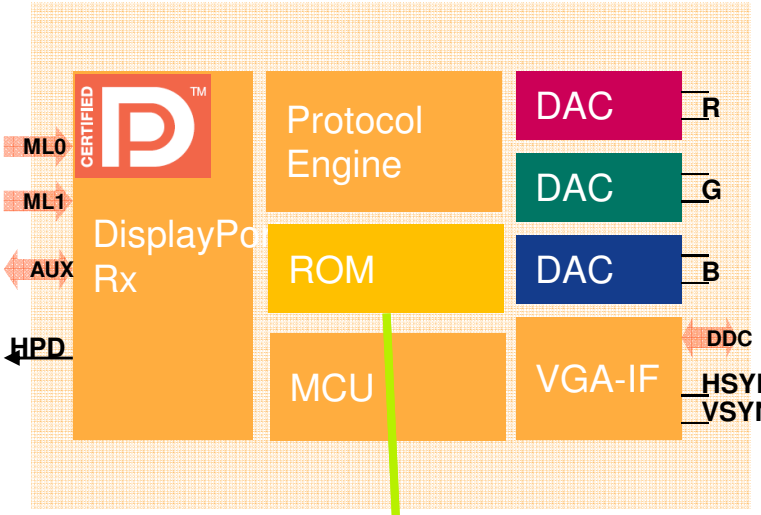


DP configuration	RBR: 1.62 Gbps	HBR: 2.70 Gbps
1 Lane	XGA, SDTV	SXGA, 1080i
2 Lanes	SXGA, 1080i	WUXGA

Sampling NOW
Production TBD

PTN3352 – Low-Power DisplayPort to VGA Bridge

- **DisplayPort receiver v1.1a**
  - 1-lane / 2-lane 2.7Gb/s / 1.62Gb/s
  - AUX channel, HPD support
- **Output**
  - Analog RGB, HSYNC, VSYNC
  - Up to 240MHz, 8bits color
  - DDC
- **Resolutions**
  - WUXGA: 1920 x 1200, 60Hz, 193MHz clock
  - UXGA: 1600 x 1200, 60Hz, 162MHz clock
  - SXGA (CRT): 1280 x 1024, 80Hz, 135MHz clock
  - SXGA: 1280 x 1024, 60Hz, 108MHz clock
  - XGA: 1024 x 768, 60Hz, 65MHz clock
  - VGA: 640 x 480, 60Hz, 25MHz clock
- Aux channel to I^2C DDC channel bridge
- 1.5V and 3.3V supply; 0 … 85 °C
- Target 400mW active @ 1920 x 1200; 10mW standby
- No support for HDCP or audio
- Support fast link training
- eDP Content Protection mechanisms
  - Support Alternate Framing
  - Support Alternate Scrambler Reset
- HVQFN40, 6x6mm, 0.5mm pitch
- ESD HBM 8kV
- 3.3V HSYNC / VSYNC outputs (min. 3.0V)
- Clock Reference Options
  - Crystal, ceramic resonator, external clock input



Does not support Flash over AUX field upgradability

DP configuration	RBR: 1.62 Gbps	HBR: 2.70 Gbps
1 Lane	XGA, SDTV	SXGA, 1080i
2 Lanes	SXGA, 1080i	WUXGA

In Development

NXP’s DisplayPort Adapter Solutions

PTN33xx for DisplayPort-DVI and HDMI dongles

Feature	PTN3360A	PTN3360B	PTN3361B	PTN3380B	PTN3360D	PTN3381B	PTN3381D
TMDS level shifters	2.5Gb/s	2.5Gb/s	1.65Gb/s	1.65Gb/s	2.5Gb/s (Deep Color HDMI)	1.65Gb/s	2.5Gb/s (Deep Color)
3.3V to 5V voltage regulator	×	×	×	✔	×	✔	✔
DDC level shifter	Pass-gate	Pass-gate	Buffer	Pass-gate	Buffer	Buffer	Buffer
HPD level shifter	1.1V inverting	3.3V non-inverting	3.3V non-inverting	3.3V non-inverting	3.3V non-inverting	3.3V non-inverting	3.3V non-inverting
Respond to I^2C HDMI dongle detect	-	-	✔ Option pin	-	-	✔ Option pin	✔ Option pin
Programmable Equalization	×	×	×	×	✔	×	✔
ESD HBM	8kV	8kV	7kV	8kV	6kV	7kV	6kV
Application	DVI / HDMI on MBD	DVI / HDMI on MBD /DVI dongle	HDMI dongle	DVI dongle	DVI / HDMI on MBD /DVI dongle	HDMI dongle	HDMI dongle

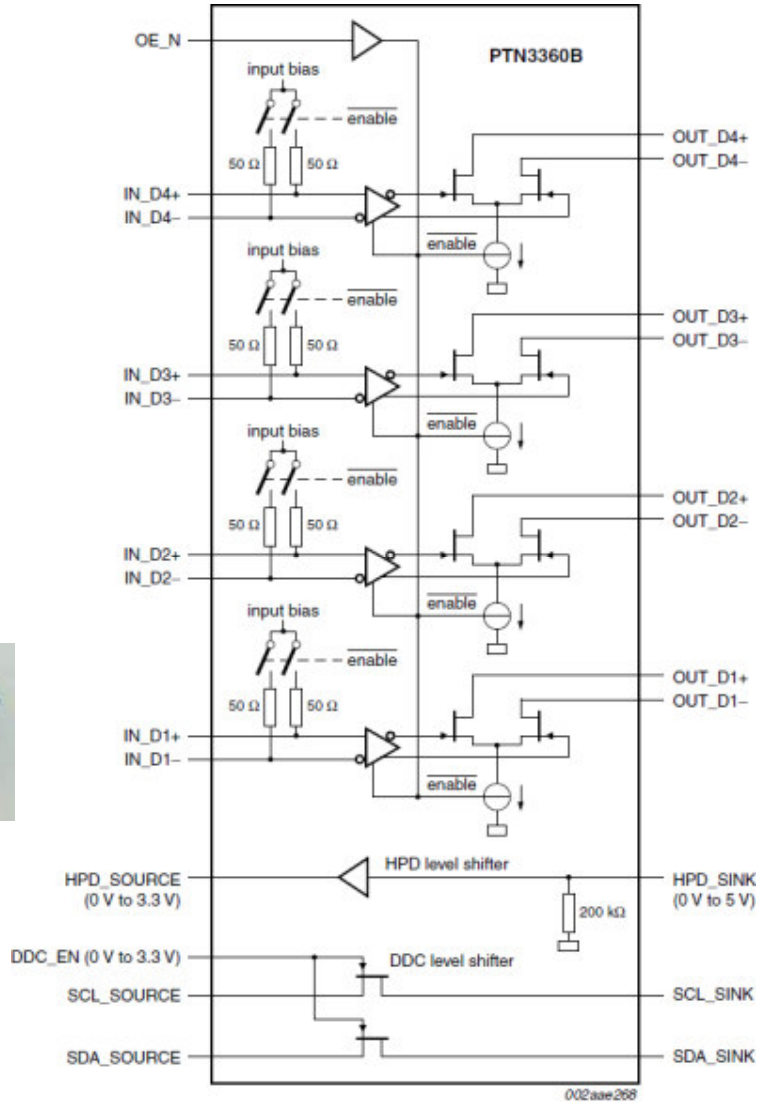
In Production

Products in Development

NOTE: I2C HDMI dongle detect is a mandatory feature for DisplayPort-HDMI dongle

PTN3360B AC-Coupled to DVI/HDMI Level Shifter

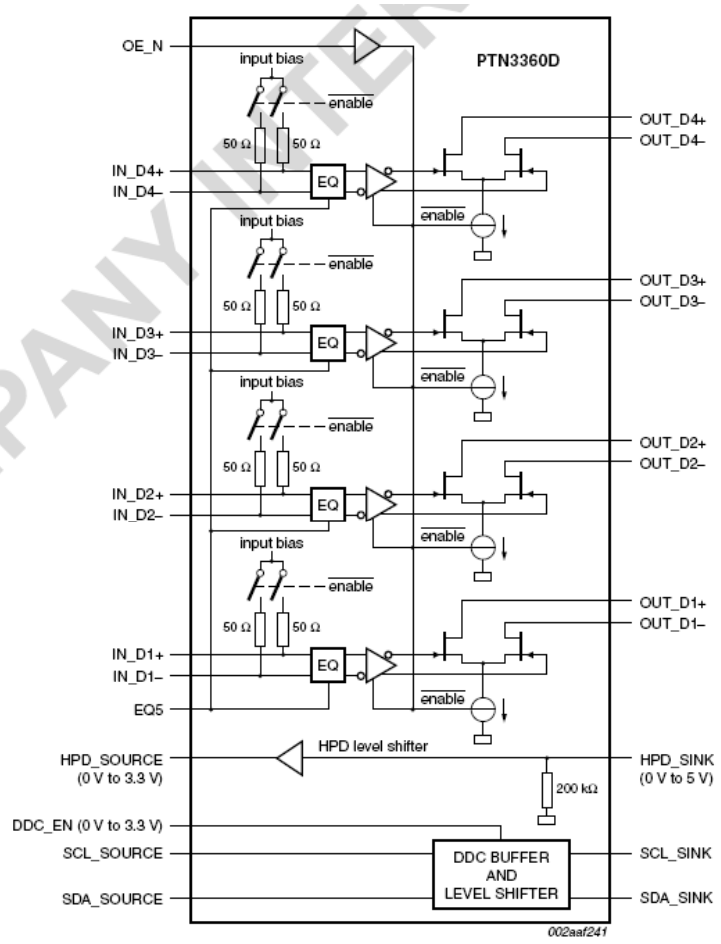
- **Inputs**
  - 4 pairs of low-swing AC-coupled differential for TX from display source to sink with integrated 50-ohm termination resistors and bias voltage
  - 1 HPD from display HPD_Sink to GMCH HPD_Source
  - 1 pair for DDC (I^2C SCL and SDA)
- **Outputs**
  - 4 pairs of TMDS outputs - up to 2.5Gb/s per lane
  - 1 pair for DDC level shifter
- Non-inverting level-shifting HPD inverter
- 3.3V ± 10% power supply
- Active 35mA typical
- -40 to +85 °C
- ESD 8kV HBM
- HVQFN 48-pin package, 7x7 mm



In Production

PTN3360D AC-Coupled to DVI/HDMI Level Shifter

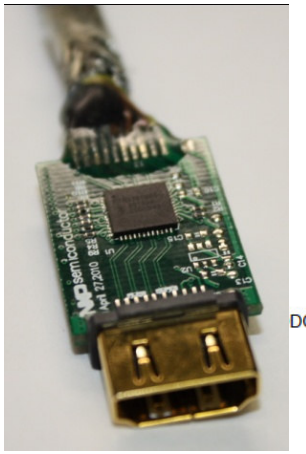
- **Inputs**
  - 4 pairs of low-swing AC-coupled differential for TX from display source to sink with integrated 50-ohm termination resistors and bias voltage
  - 1 HPD from display HPD_Sink to GMCH HPD_Source
  - 1 pair for DDC (I^2C SCL and SDA)
- **Outputs**
  - 4 pairs of TMDS outputs - up to 2.5Gb/s per lane
  - Supports HDMI Deep Color at 10bits/color
  - 1 pair for DDC level shifter / buffer
- Programmable equalizer
- Non-inverting level-shifting HPD inverter
- 3.3V ± 10% power supply
- Active 35mA typical
- -40 to +85 °C
- ESD 6kV HBM
- HVQFN 48-pin package, 7x7 mm

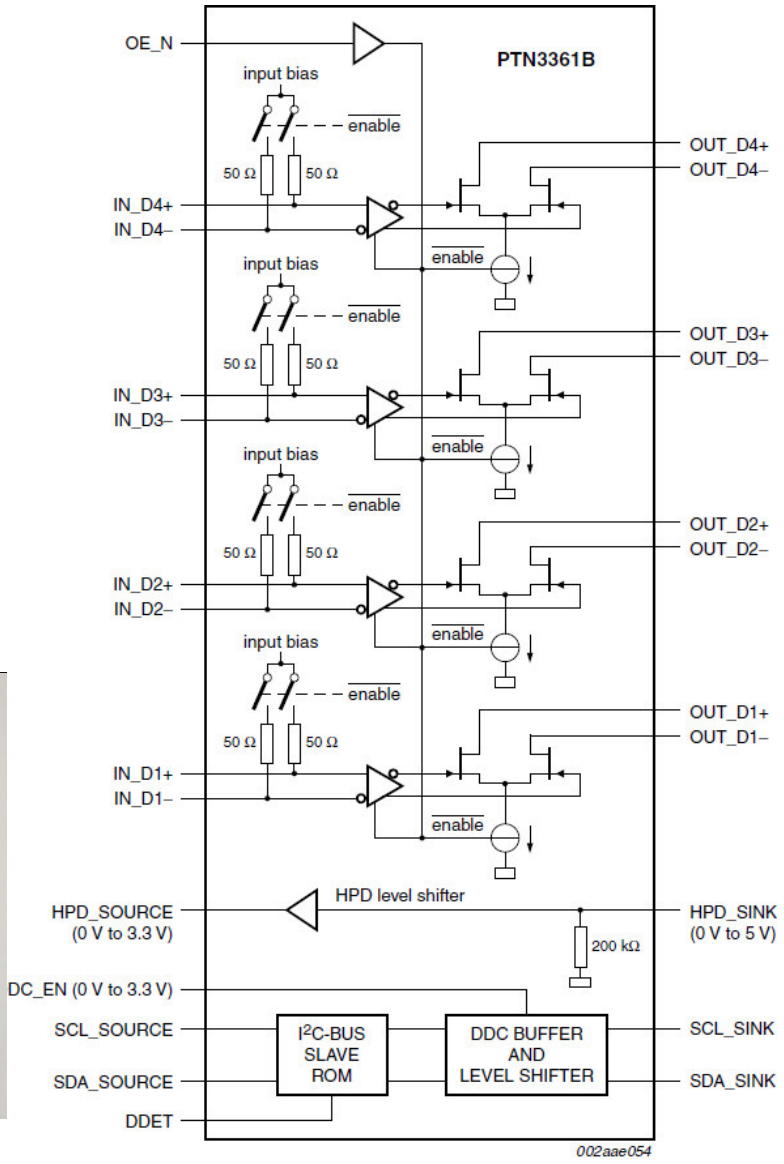


In Production

PTN3361B AC-Coupled to DVI/HDMI Level Shifter

- **Inputs**
  - 4 pairs of low-swing AC-coupled differential for TX fron display source to sink with integrated 50-ohm terminati resistors and bias voltage
  - 1 HPD from display HPD_Sink to north bridge HPD_S
  - 1 pair for DDC (I²C SCL and SDA)
- **Outputs**
  - 4 pairs of TMDS outputs - Up to 1.65Gb/s per lane
  - 1 pair for DDC buffer and level shifter
  - Optional I²C-based HDMI dongle detect
- Respond to HDMI dongle detect via I²C (option pin)
  - Mandatory feature for DisplayPort-HDMI dongle
- 3.3V ± 10% power supply
- Active current consumption t.b.d.
- -40 to +85 °C
- ESD 8kV HBM (target)
- PTN3361BBS: HVQFN-48, 7x7 mm
- **Suitable for DisplayPort-HDMI Dongle**





In Production

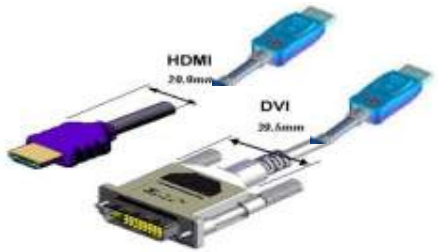
PTN3361B - HDMI Dongle Detect via I²C

Multi-mode Display Source outputs DVI? HDMI?

- When connected to a DVI dongle or HDMI dongle, how does a multi-standard source determine what display interface to transmit?
  - Pin 13 = HIGH means a dongle is attached
  - Source reads at I²C address 81h
    - If DVI dongle, no response from dongle
    - If HDMI dongle, dongle returns a predetermined character sequence

Table 4. DisplayPort - HDMI Adaptor Detection ROM content

Internal pointer offset	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Data	44	50	2D	48	44	4D	49	20	41	44	41	50	54	4F	52	04

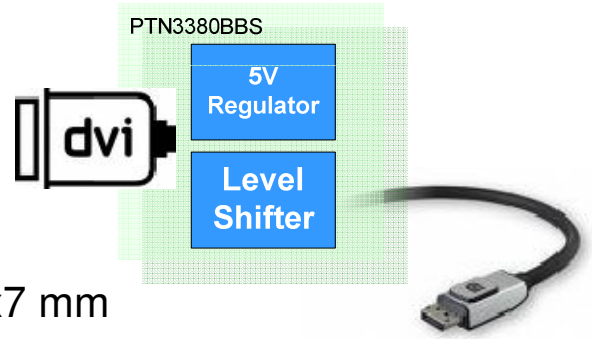


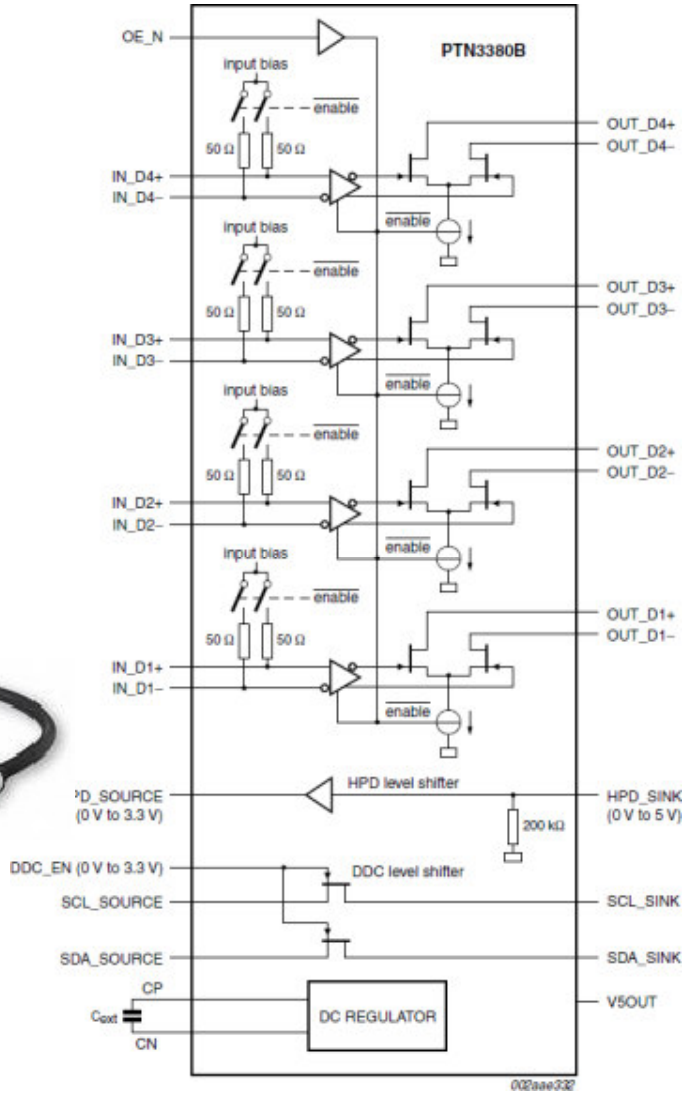
DVI 1.0/HDMI Mode		DisplayPort Pins
Channel 2	↔	Main Link Lane 0
Channel 1	↔	Main Link Lane 1
Channel 0	↔	Main Link Lane 2
Channel Clock	↔	Main Link Lane 3
DDC Clock	↔	AUX CH+
DDC Data	↔	AUX CH-
DP_PWR	↔	DP_PWR (+3.3V)
Hot Plug Detect	↔	Hot Plug Detect
Cable Adaptor Detect (Optional)		Pin 13
CEC (HDMI cable adaptor only)		Pin 14

- PTN3361B supports HDMI dongle detect via I²C
  - Option pin DDET tied LOW for DVI dongle
  - Option pin DDET tied HIGH for HDMI dongle

PTN3380B AC-Coupled to DVI/HDMI Level Shifter & 3.3V/5V Regulator

- **Inputs**
  - 4 pairs of low-swing AC-coupled differential for TX from display source to sink with integrated 50-ohm termination resistors and bias voltage
  - 1 HPD from display HPD_Sink to GMCH HPD_Source
  - 1 pair for DDC (I^2C SCL and SDA)
- **Outputs**
  - 4 pairs of TMDS outputs - up to 1.65Gb/s per lane
  - 1 pair for DDC level shifter
- Non-inverting level-shifting HPD inverter
- 3.3V ± 10% power supply
- Active Current TBD
- -40 to +85 °C
- ESD 8 kV HBM (target)
- HWQFN 48-pin package, 7x7 mm
- PTN3380B = PTN3360B + Integrated 3.3V to 5V Voltage Regulator
  - **Integrated solution for Low-cost DP-DVI Dongle; Lowest system BOM**
  - 3.3V to 5V voltage regulator supports 55mA load

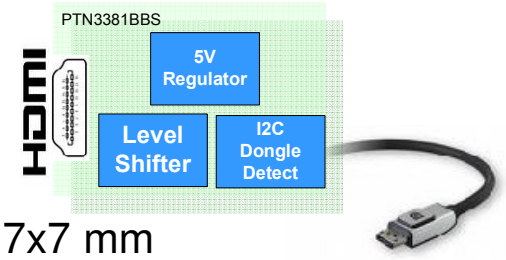


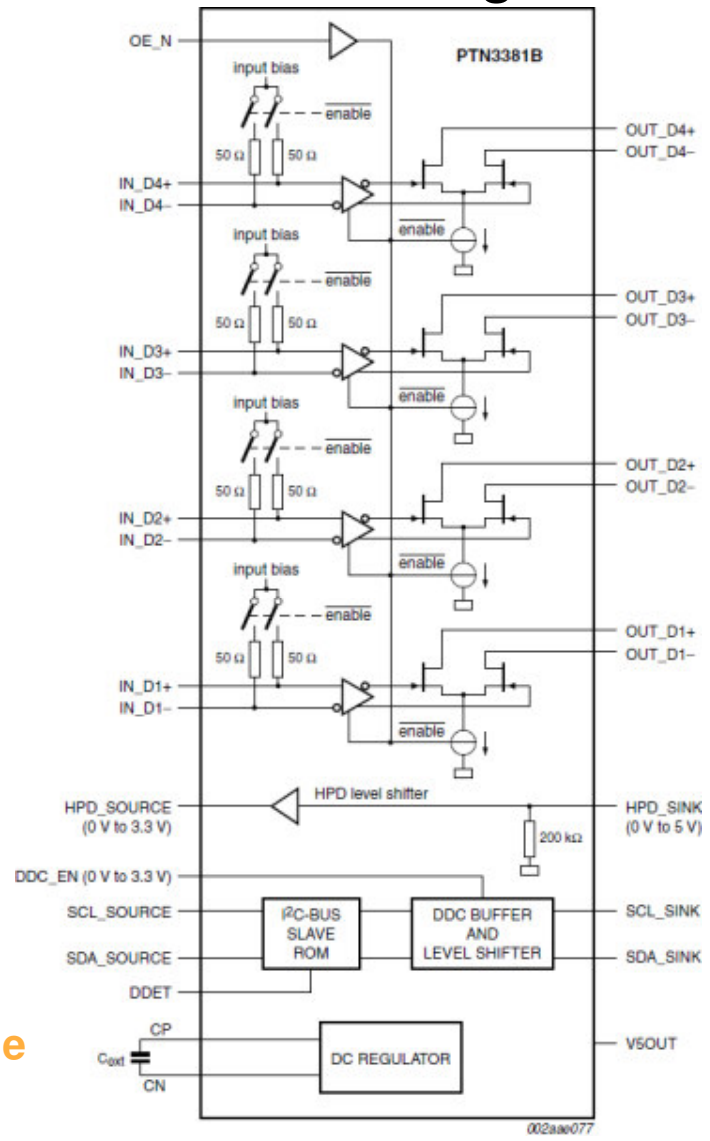


In Production

PTN3381B HDMI Level Shifter w/ DDC Buffer & 3.3V/5V Regulator

- **Inputs**
  - 4 pairs of low-swing AC-coupled differential for TX from display source to sink with integrated 50-ohm termination resistors and bias voltage
  - 1 HPD from display HPD_Sink to GMCH HPD_Source
  - 1 pair for DDC (I^2C SCL and SDA)
- **Outputs**
  - 4 pairs of TMDS outputs - Up to 1.65Gb/s per lane
  - 1 pair for DDC level shifter
  - Optional I^2C-based HDMI dongle detect
- Respond to HDMI dongle detect via I^2C (option pin)
  - Mandatory feature for DisplayPort-HDMI dongle
- 3.3V ± 10% power supply
- 0 to +70 °C
- ESD 8kV HBM (target)
- PTN3381BBS: HVQFN-48, 7x7 mm
- PTN3381B = PTN3361B + Integrated 3.3V to 5V Voltage Regulator
  - **Integrated solution for Low-cost DP-HDMI Dongle**
  - 3.3V to 5V voltage regulator (55mA)





Sampling NOW

DPDVI Reference Design

NXP DP-DVI dongle with PTN3360B or PTN3360D or PTN3361B or PTN3380B

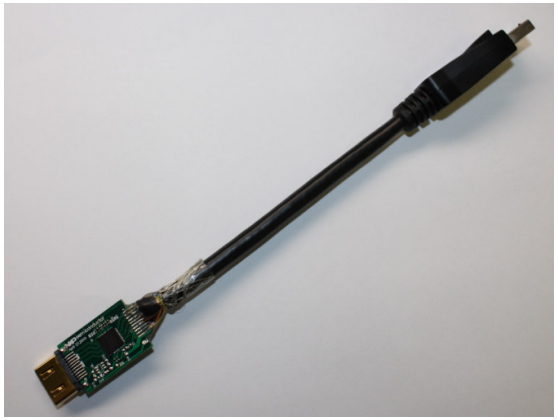
- Availability: NOW
- Hardware:
  - Hardware ready for both PTN3360B/60D/61B and PTN3380B (stuff option)
  - Form factor optimized as a production-ready dongle
  - Reflects best practices in schematics and layout
  - Reflects best-in-class BOM cost
  - Constitutes a reference design of PTN3360B/D, PTN3361B, PTN3380B

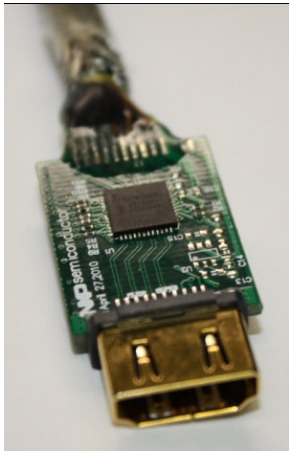
- Contents
  - Full schematic and layout
  - Bill of Materials
  - Design and layout guidelines for optimal performance and EMC
- Purposes
  1. Customer reference design
  2. PTN3360/3361/3380 interop testing
  3. Trade show demos

DPHDMI Reference Design

NXP DP-HDMI dongle with PTN3361B or PTN3361D or PTN3381D

- Availability: Soon
- Hardware:
  - Hardware ready for both PTN3361B, PTN3361D, and PTN3381B (stuff option)
  - Form factor optimized as a production-ready dongle
  - Reflects best practices in schematics and layout
  - Reflects best-in-class BOM cost
  - Constitutes a reference design of PTN3361B, PTN3361D and PTN3381D





- Contents
  - Full schematic and layout
  - Bill of Materials
  - Design and layout guidelines for optimal performance and EMC
- Purposes
  1. Customer reference design
  2. PTN3361/3381 interop testing
  3. Trade show demos

PTN3360/1, PTN3380/1 Schedule

PTN3360BBS	
✓ PTN3360BBS Production	DONE
✓ DP-DVI Reference Design (PTN3360)	AVAILABLE
✓ DP-DVI Reference Design Interoperability Tests (PTN3360)	AVAILABLE
PTN3361BBS	
✓ PTN3361BBS Production	DONE
✓ DP-DVI Reference Design (PTN3361)	AVAILABLE
✓ DP-DVI Reference Design Interoperability Tests (PTN3361)	AVAILABLE
▸ DP-HDMI Reference Design (PTN3361)	2H, 2010
▸ DP-HDMI Interoperability Tests (PTN3361)	2H, 2010
PTN3360DBS	
✓ PTN3360DBS Production	DONE
PTN3380BBS	
✓ PTN3380BBS Production	DONE
✓ DP-DVI Reference Design (PTN3380)	AVAILABLE
✓ DP-DVI Reference Design Interoperability Tests (PTN3380)	AVAILABLE
PTN3381BBS	
✓ PTN3381BBS Sampling	AVAILABLE
▸ PTN3381BBS Production	2H, 2010

APPENDIX: Firmware Update via Host Flash-over-AUX Feature

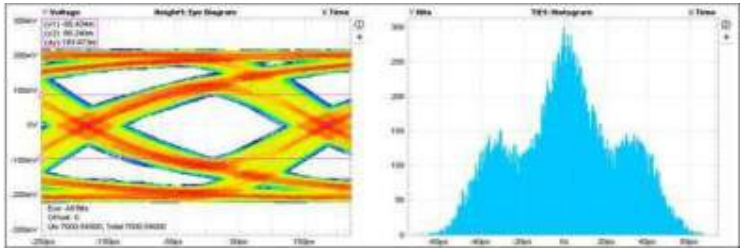
Firmware updater Tested on these PCs

Computer	OS	GPU	Driver Version	VBIOS Version	Flash over AUX Status
Dell Latitude E5400	Vista SP1	Mobile Intel 4 Series Express Chipset	8.15.10.2018	1659	Working
Dell Dimension 4700	WinXP SP2	NVIDIA GeForce 9400GT	195.62	62.94.4A.00.00	Working
MacBook Pro	OS X 10.5.6	NVIDIA GeForce 9400M	OS X 10.5.6	OS X 10.5.6	Not available for Mac OS yet
Lenovo W700	Vista SP1	NVIDIA Quadro FX 2700M	195.62	62.94.45.00.10	Working
HP ProBook 5310m	WinXP SP3	Mobile Intel 4 Series Express Chipset	6.14.10.2018	1785	Working
Dell Studio 14z	Vista SP1	NVIDIA GeForce 9400M	195.62	62.79.5B.00.05	Working
Lenovo 3000H Series	Vista SP1	ATI Radeon HD3470	10.3 (8.01.01.1010)	010.088.000.031	Working
Intel Calpella Customer Reference Board (CRB)	Win7	Intel HD Graphics	8.15.10.2018	1960	Working

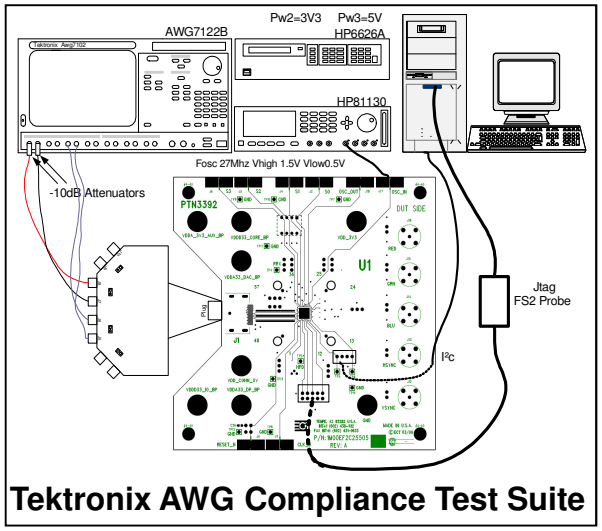
APPENDIX: Compliance and EMI Test Results

PTN3392 DisplayPort PHY Compliance Test

- Jitter and height measurement with RBR & HBR (Gain 0 to 7) @ -5°C, 25°C, 85°C
  - @ 2MHz
  - @ 10MHz
  - @ 20MHz
  - @ 100MHz



Input measurement HBR @ 100MHz



Tektronix AWG Compliance Test Suite

AWG pattern
Amplitude AWG 700mV + attenuator 10dB

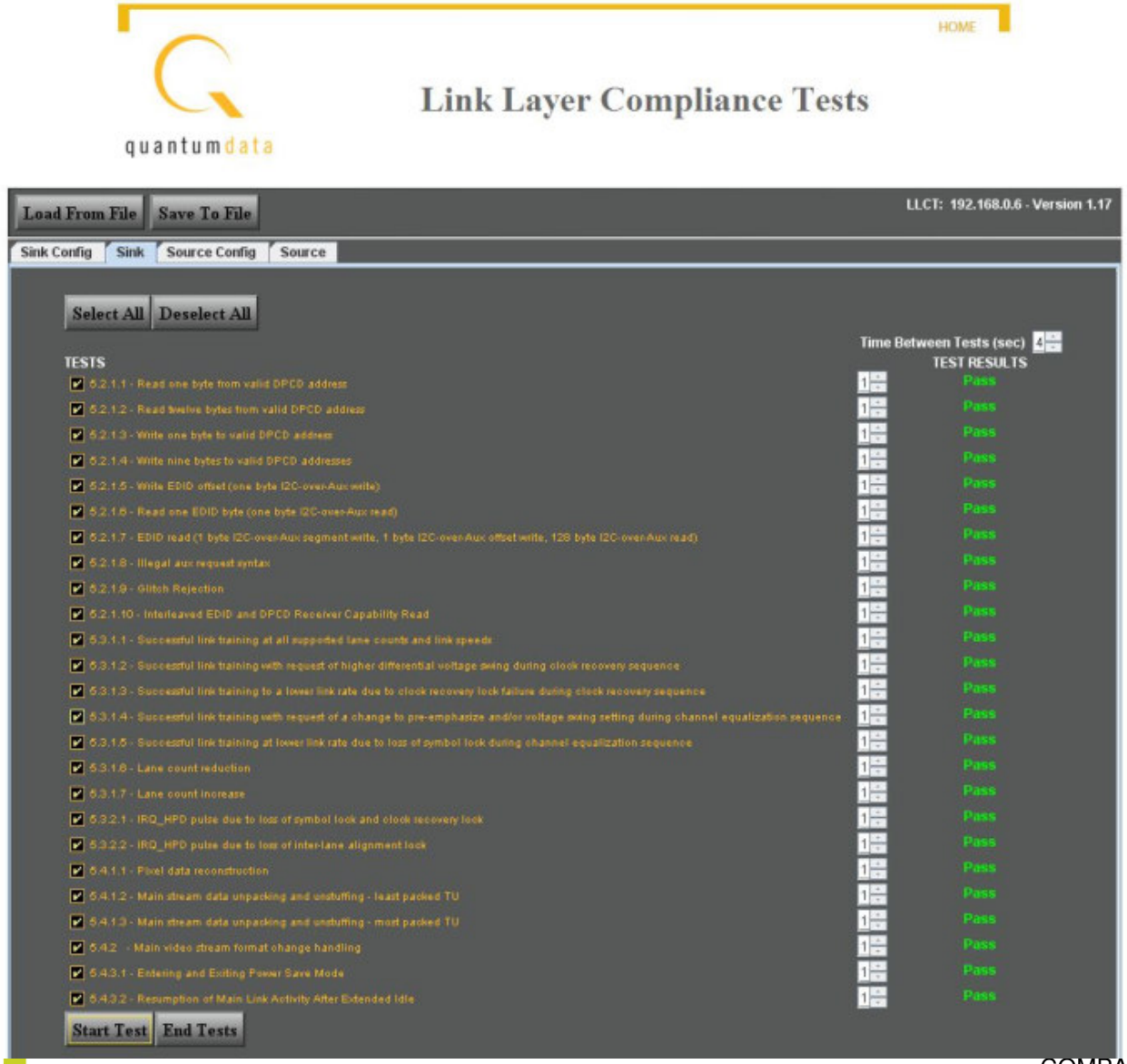
	Lane 0			Lane 1		
Speed	-5 °C	25 °C	85 °C	-5 °C	25 °C	85 °C
RBR 2 MHz	PASS	PASS	PASS	PASS	PASS	PASS
RBR 10 MHz	PASS	PASS	PASS	PASS	PASS	PASS
RBR 20 MHz	PASS	PASS	PASS	PASS	PASS	PASS
HBR 2 MHz	PASS	PASS	PASS	PASS	PASS	PASS
HBR 10 MHz	PASS	PASS	PASS	PASS	PASS	PASS
HBR 20 MHz	PASS	PASS	PASS	PASS	PASS	PASS
HBR 100 MHz	PASS	PASS	PASS	PASS	PASS	PASS

Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR RBR	2 MHz	10^{12}	1000	HBR=370s RBR=620s	0
HBR RBR	10 MHz	10^{11}	100	HBR=37s RBR=62s	+350ppm +350ppm
HBR RBR	20 MHz	10^{11}	100	HBR=37s RBR=62s	0
HBR	100 MHz	10^{11}	100	HBR=37s	0

To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^{11} bits at HBR = 370ps/UI * 10^{11} UI = 37 seconds

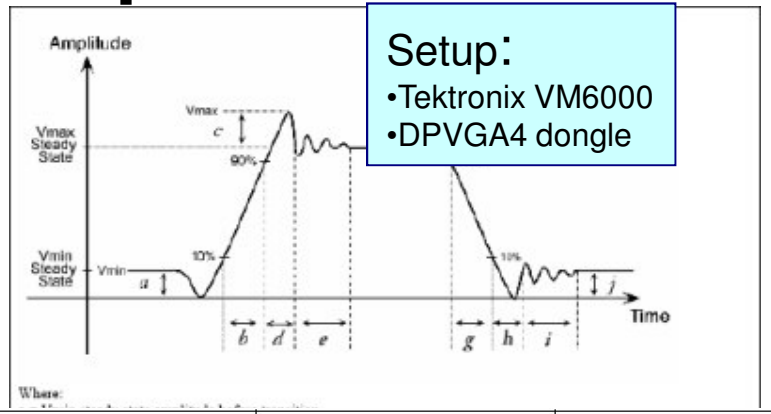
PTN3392 DP Link Layer Compliance Tests



PTN3392 VSIS v1.2 VGA Compliance Tests

- Resolutions tested * video filter optimization TBD
  - •VGA 640x480@60Hz, 8 bits per color, 25.175MHz clock
  - •SVGA 800x600@60Hz, 8 bits per color, 40MHz clock
  - •XGA 1024x768@60Hz, 8 bits per color, 65MHz clock
  - •SXGA 1280x1024@60Hz, 8 bits per color, 108MHz clock
  - •SXGA 1280x1024@85Hz, 8 bits per color, 135MHz clock
  - •UXGA 1600x1200@60Hz, 8 bits per color, 162MHz clock
  - •WUXGA 1920x1200@60Hz, 8 bits per color, Reduced Blanking, 154 MHz clock
  - •WUXGA 1920x1200@60Hz, 6 bits per color, 193 MHz clock

Setup:
- •Tektronix VM6000
- •DPVGA4 dongle



SUMMARY:	Status
H Sync	PASS
V Sync	PASS
Color Bars	PASS
Ch-Ch Mismatch	PASS
Ch-Ch Skew	PASS
Luma Levels	PASS
Noise Inj Ratio	PASS
Linearity	PASS
Video Transient	PASS
H Sync Jitter	PASS

	Value	Comment
Max Luminance Voltage Input Data = (FFh)	0.700 Volts +0.070 /-0.035 volts	DC Measurement. See note (a) and (d).
Min Luminance voltage Input Data = (00h)	0.000 Volts	DC Measurement. See note (a) and (d).
Video Channel Rise/Fall Time Max	25% of minimum pixel clock period	See notes (b), (e) and (g).
Maximum Settling Time after overshoot/undershoot	30% of minimum pixel clock period averaged over 100 waveforms to 5% final full-scale value.	See notes (b).
Monotonic	Yes	Definition in section 2.6
Resolution	1 LSB	
Integral Linearity Error	+/- 1 LSB	Definition in section 2.6
Differential Linearity Error	+/- 1 LSB	Definition in section 2.6
Video Channel to Video Channel Mismatch	6% of any video output voltage over the full voltage range	See notes (f).

Hsync and Vsync (VSIS Table 2.1)	VSIS Requirement
Driver Logic level "1"	2.4 V min., 5.5 V max
Driver Logic level "0"	0.0 V min., 0.5 V max
Driver High Level Output Current	-8mA
Driver Low Level Output Current	+8mA
Fall Time Max	80% of min. pixel clock period
Rise Time Max	80% of min. pixel clock period
Monotonic Rise/Fall Time Voltage Range	0.5 - 2.4 V
Overshoot/Undershoot max	30% of high level signal voltage range no excustions allowed in the 0.5-2.4 volt range
Jitter (Measured between Hsyncs) max	15% of p-p of clock period

Video Signals (VSIS table 2.2)	Value
Video Noise injection ratio	+/- 2.5 % of Max Luminance Voltage
Video Channel to Video Channel Output Skew	50% of minimum pixel clock period
Overshoot/Undershoot	+/-12% of step function voltage level over the full voltage range

PTN3392 VGA DAC INL Measurement Update

- Set up: Tektronix VM6000
- DPVGA4 dongle
- Status: Previously failing resolutions NOW PASS
- Datasheet updated to reflect INL of <+/-1 LSB

- DAC INL previously failing at some resolutions
  - Determined that VM6000 has linearity anomalies for given sensitivity and offset settings that impact results
  - Sensitivity changed from 96mV/div to 80 mV /div
  - Measurement averages set to “3”, waveform averages set to 500 to compensate for oscilloscope noise effects Measurements retaken with results below. Previously failing resolutions highlighted in dark orange

Table 12. DAC characteristics

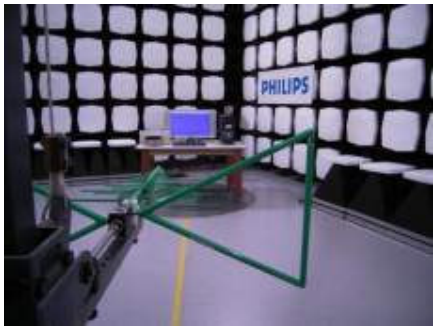
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{res(DAC)}$	DAC resolution		-	-	8	bit
f_{clk}	clock frequency		-	-	240	MHz
$\Delta I_{o(DAC)}$	DAC-to-DAC output current matching		-	-	4	%
INL	integral non-linearity		−1	±0.5	+1	LSB
DNL	differential non-linearity		−1	-	+1	LSB
$V_{O(compl)}$	DAC output voltage compliance		0	-	1.25	V
C_o	DAC output capacitance		-	3.5	-	pF
$\alpha_{ct(DAC)}$	DAC crosstalk	between DAC outputs	-	−54	-	dB

Resolution	Measured INL (LSB) **NOW ALL PASS!!**	Previous Results
640x480@60Hz	< +/- 1	Fail
800x600@60Hz	< +/- 1	Pass
1024x768@60Hz	< +/- 1	Pass
1280x1024@60Hz	< +/-1	Pass
1600x1200@60Hz	< +/-1	Fail
1920x1200@60RB	< +/-1	Fail
6b 1920x1200@60Hz	< +/-1	Pass

DPVGA4 EMI Test Results and Findings

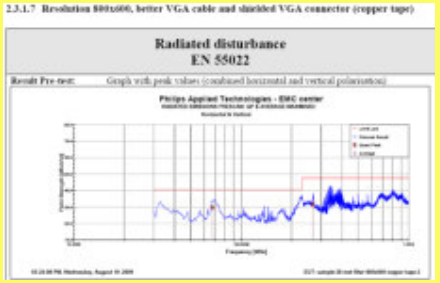
EMI Chamber Tests

- Test Setup
  - DPVGA4 Prototype Dongle with PTN3392
  - Dell Latitude E6500 with power supply and mouse
  - Scrolling “H” pattern
  - Philips Brilliance 200P LCD monitor
  - Resolutions Tested
    - 800 x 600; 1600 x 1200, 1280 x 1024
- EMI Test Findings
  - **PASS** CISPR22B without metal shielding (however, without the desired 3-6dB margin)
  - PI-filter is indeed not necessary for EMI reasons
    - However, RGB filtering needed to pass VSIS

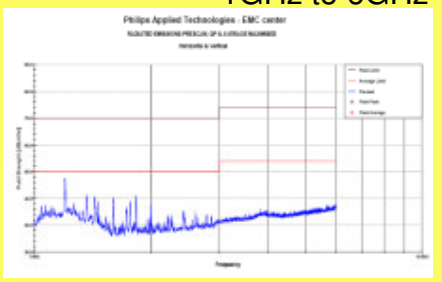


Semi-Anechoic Chamber

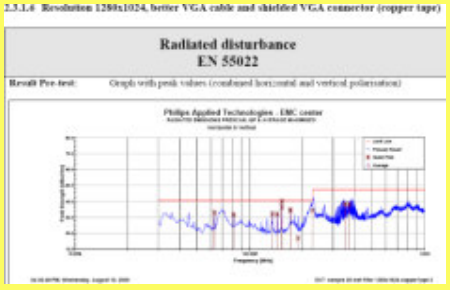
30MHz to 1GHz **Resolution: 800 x 600** 1GHz to 6GHz

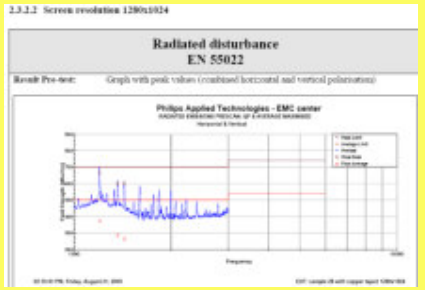


30MHz to 1GHz **Resolution: 1600 x 1200** 1GHz to 6GHz



30MHz to 1GHz **Resolution: 1280 x 1024** 1GHz to 6GHz

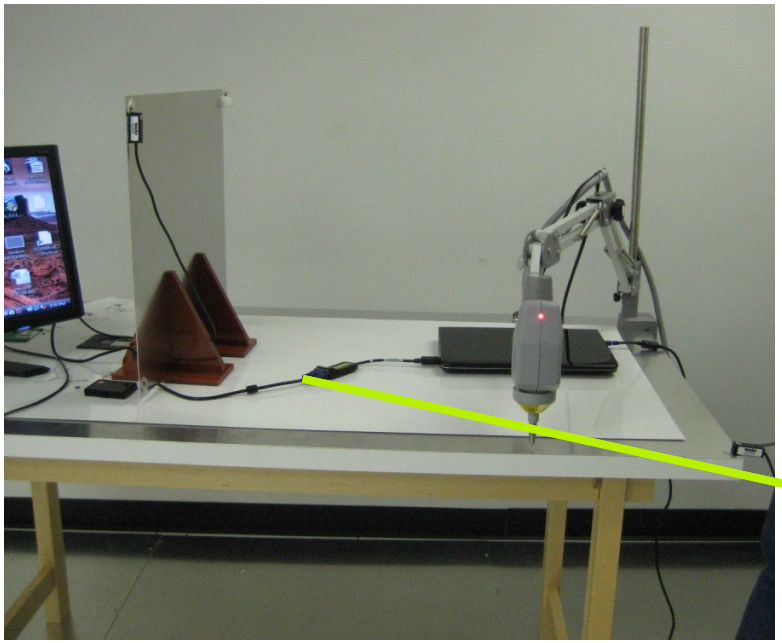




Recommend metal tape around VGA connector or metal cage

DPVGA4 IEC61000-4-2 ESD Tests

Test Performed	Test date	Level	Criteria/Result	Comment	
ESD – Enclosure	2010/02/19	4	B / Pass	Notes Deviations	Pass



Pass without external
ESD Protection Devices!

DPVGA4 IEC61000-4-2 ESD Tests

Indirect Discharges (to Coupling Planes)	Positive Polarity (kV)				Negative Polarity (kV)			
Contact Mode	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**Level 1**	**Level 2**	**Level 3**	**Level 4**
	2	**4**	**6**	**8**	**2**	**4**	**6**	**8**
VCP located 10cm from the front, rear, left, and right sides of the EUT	X	X	X	X	X	X	X	X
HCP located 10cm from the front, rear, left, and right sides of the EUT	X	X	X	X	X	X	X	X
Direct Discharges (to the EUT)	**Positive Polarity (kV)**				**Negative Polarity (kV)**			
Contact Mode	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**Level 1**	**Level 2**	**Level 3**	**Level 4**
	2	**4**	**6**	**8**	**2**	**4**	**6**	**8**
VGA shell	X	X	X	X	X	X	X	X
Display Port shell	X	X	X	X	X	X	X	X
Air Discharge Mode	**Positive Polarity (kV)**				**Negative Polarity (kV)**			
Contact Mode	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**Level 1**	**Level 2**	**Level 3**	**Level 4**
	2	**4**	**8**	**15**	**2**	**4**	**8**	**15**
VGA shell	X	X	X	X	X	X	X	Note 3
Display Port shell	X	X	X	X	X	X	X	Note 3

Note 1: An “X” indicates that the EUT continued to operate as intended

Note 2: ND: No discharges was possible due to lack of discharge path to ground from test point.
HCP: Horizontal Coupling Plane,
VCP: Vertical Coupling Plane.

Note 3: Image disappeared but returned to normal by itself. Criterion B.

Note 4: 10 positive and 10 negative discharges applied to each side of EUT

APPENDIX: Interoperability Test Suites

DisplayPort Sources

Computer Model	Type	Graphics Card	OS	Graphics Driver
Dell Latitude E5400	Laptop	Mobile Intel 4 Series Express Chipset	Vista SP1	8.15.10.2018
Dell Dimension 4700	Desktop GPU Card	NVIDIA GeForce 9400GT	WinXP SP2	195.62
MacBook Pro	Laptop	NVIDIA GeForce 9400M	OS X 10.5.6	OS X 10.5.6
Lenovo W700	Laptop	NVIDIA Quadro FX 2700M	Vista SP1	195.62
HP ProBook 5310m	Laptop	Mobile Intel 4 Series Express Chipset	WinXP SP3	
Dell Studio 14z	Laptop	NVIDIA GeForce 9400M	Vista SP1	195.62
Lenovo 3000H Series	Desktop GPU Card	ATI Radeon HD3470	Vista SP1	10.3 (8.01.01.1010)
Calpella CRB	Laptop	Intel HD Graphics	Win7	8.15.10.2018
Lenovo 3000H Series	Desktop GPU Card	ATI Radeon HD5750	Vista SP1	10.1 (8.01.01.994)

Sinks (Monitors used w/ VGA)

Monitor Model	Highest Resolution
PHILIPS 190B	1280x1024
ACER X213W	1680x1050
DELL 1905FP	1280x1024
DELL 2408WFP	1920x1200
DELL 1908FP	1280x1024
SAMSUNG LT4065F	1920x1080

VGA Cables Used

Cable Length
6ft
15ft
50ft
100ft

Interoperability Test Matrix

Sink	Source	Firmwa	Test Name	Cable Length
2408WFP	ATI HD3650	1.07	800x600 @ 60	6ft
2408WFP	ATI HD3650	1.07	800x600 @ 72	6ft
2408WFP	ATI HD3650	1.07	800x600 @ 75	6ft
2408WFP	ATI HD3650	1.07	1024x768 @ 60	6ft
2408WFP	ATI HD3650	1.07	1024x768 @ 70	6ft
2408WFP	ATI HD3650	1.07	1024x768 @ 75	6ft
2408WFP	ATI HD3650	1.07	1280x960 @ 60Hz	6ft
2408WFP	ATI HD3650	1.07	1280x960 @ 75Hz	6ft
2408WFP	ATI HD3650	1.07	1280 x1024 @ 60	6ft
2408WFP	ATI HD3650	1.07	1280 x1024 @ 75	6ft
2408WFP	ATI HD3650	1.07	1360x768 @ 60	6ft
2408WFP	ATI HD3650	1.07	1600x1200 60	6ft
2408WFP	ATI HD3650	1.07	1920x1200 @ 60	6ft
2408WFP	ATI HD3650	1.07	Shutdown	6ft
2408WFP	ATI HD3650	1.07	Restart	6ft
2408WFP	ATI HD3650	1.07	Hibernate	6ft
2408WFP	ATI HD3650	1.07	HPD	6ft
2408WFP	ATI HD3650	1.07	Standby	6ft
2408WFP	ATI HD3650	1.07	Timeout	6ft
2408WFP	ATI HD3650	1.07	Single	6ft
2408WFP	ATI HD3650	1.07	Clone	6ft
2408WFP	ATI HD3650	1.07	Extended	6ft
2408WFP	ATI HD3650	1.07	Resolution Fig of Merit	6ft
2408WFP	ATI HD3650	1.07	Overall Fig of Merit	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	800x600 @ 60	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	800x600 @ 72	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	960x600 @ 60	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	960x600 @ 75	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1024x768 @ 60	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1152x864 @ 60Hz	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1152x864 @ 75Hz	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1280x768 @ 60Hz	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1280x768 @ 75Hz	6ft

Sink	Source	Firmwa	Test Name	Cable Leng
2408WFP	Dell Laptop Intel	1.07	800x600 @ 60	15ft
2408WFP	Dell Laptop Intel	1.07	800x600 @ 75	15ft
2408WFP	Dell Laptop Intel	1.07	1280 x1024 @ 60	15ft
2408WFP	Dell Laptop Intel	1.07	1280 x1024 @ 75	15ft
2408WFP	Dell Laptop Intel	1.07	1920x1200 @ 60	15ft
2408WFP	Dell Laptop Intel	1.07	800x600 @ 60	50ft
2408WFP	Dell Laptop Intel	1.07	800x600 @ 75	50ft
2408WFP	Dell Laptop Intel	1.07	1280 x1024 @ 60	50ft
2408WFP	Dell Laptop Intel	1.07	1280 x1024 @ 75	50ft
2408WFP	Dell Laptop Intel	1.07	1920x1200 @ 60	50ft
2408WFP	Dell Laptop Intel	1.07	800x600 @ 60	100ft
2408WFP	Dell Laptop Intel	1.07	800x600 @ 75	100ft
2408WFP	Dell Laptop Intel	1.07	1024x768 @ 60	100ft
2408WFP	Dell Laptop Intel	1.07	1024x768 @ 75	100ft
2408WFP	Dell Laptop Intel	1.07	1280 x1024 @ 60	100ft
2408WFP	Dell Laptop Intel	1.07	1280 x1024 @ 75	100ft
2408WFP	Dell Laptop Intel	1.07	1440x900 @ 60	100ft
2408WFP	Dell Laptop Intel	1.07	1920x1200 @ 60	100ft
1905FP	Macbook Pro GF 9400	1.07	VGA Cable, no I2C	6ft
1905FP	Macbook Pro GF 9400	1.07	VGA Cable, SDA to GND	6ft
1905FP	Macbook Pro GF 9400	1.07	VGA Cable, SCL to GND	6ft
190B	Dell nVidia	1.07	800x600 @ 56	6ft
190B	Dell nVidia	1.07	800x600 @ 60	6ft
190B	Dell nVidia	1.07	800x600 @ 72	6ft
190B	Dell nVidia	1.07	800x600 @ 75	6ft
190B	Dell nVidia	1.07	1024x768 @ 60	6ft
190B	Dell nVidia	1.07	1024x768 @ 70	6ft
190B	Dell nVidia	1.07	1024x768 @ 75	6ft
190B	Dell nVidia	1.07	1152x864 @ 75Hz	6ft
190B	Dell nVidia	1.07	1280x960 @ 60Hz	6ft
190B	Dell nVidia	1.07	1280 x1024 @ 60	6ft
190B	Dell nVidia	1.07	1280 x1024 @ 75	6ft
190B	Dell nVidia	1.07	Shutdown	6ft

Resolution Figure of Merit

Definition: Resolution Figure of Merit =
Average score of all resolution tests

- Each source-to-sink combination may have a unique # and list of resolutions
- Each test score has equal weight

– Each test gets a score on a scale of 1 to 10.
  - 1 = failed test, not user fixable
    – E.g. Permanent Blinking, blanking, flashing
  - 5 = fixable or occasional flaw
    – E.g. by changing resolution image may be restored
  - 10 = pass
    – Perfect image

– Interpretation Guide
  - 10 = Perfect (our goal)
  - Score ≥ 9.9 acceptable
  - 1 = Total Failure

Sink	Source	Firmwa	Test Name	Cable Length
2408WFP	ATI HD3650	1.07	800x600 @ 60	6ft
2408WFP	ATI HD3650	1.07	800x600 @ 72	6ft
2408WFP	ATI HD3650	1.07	800x600 @ 75	6ft
2408WFP	ATI HD3650	1.07	1024x768 @ 60	6ft
2408WFP	ATI HD3650	1.07	1024x768 @ 70	6ft
2408WFP	ATI HD3650	1.07	1024x768 @ 75	6ft
2408WFP	ATI HD3650	1.07	1280x960 @ 60Hz	6ft
2408WFP	ATI HD3650	1.07	1280x960 @ 75Hz	6ft
2408WFP	ATI HD3650	1.07	1280 x1024 @ 60	6ft
2408WFP	ATI HD3650	1.07	1280 x1024 @ 75	6ft
2408WFP	ATI HD3650	1.07	1360x768 @ 60	6ft
2408WFP	ATI HD3650	1.07	1600x1200 60	6ft
2408WFP	ATI HD3650	1.07	1920x1200 @ 60	6ft
2408WFP	ATI HD3650	1.07	Shutdown	6ft
2408WFP	ATI HD3650	1.07	Restart	6ft
2408WFP	ATI HD3650	1.07	Hibernate	6ft
2408WFP	ATI HD3650	1.07	HPD	6ft
2408WFP	ATI HD3650	1.07	Standby	6ft
2408WFP	ATI HD3650	1.07	Timeout	6ft
2408WFP	ATI HD3650	1.07	Single	6ft
2408WFP	ATI HD3650	1.07	Clone	6ft
2408WFP	ATI HD3650	1.07	Extended	6ft
2408WFP	ATI HD3650	1.07	Resolution Fig of Merit	6ft
2408WFP	ATI HD3650	1.07	Overall Fig of Merit	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	800x600 @ 60	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	800x600 @ 72	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	960x600 @ 60	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	960x600 @ 75	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1024x768 @ 60	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1152x864 @ 60Hz	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1152x864 @ 75Hz	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1280x768 @ 60Hz	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1280x768 @ 75Hz	6ft

Overall Figure of Merit

Definition: Overall Figure of Merit =
Average score of all interop tests

- Each source-to-sink combination may have a unique # and list of all tests
- Each test score has equal weight
- Tests include Hotplug, EDID, Clone, Primary, etc.. AND all resolution tests

– Each test gets a score on a scale of 1 to 10.
  - 1 = permanently failed test, not user fixable
    – E.g. Permanent Hot-plug fail, simple primary no image
  - 2 = largely failed test
    – E.g. 7 out of 8 Hot-plugs fail
  - 5 = fixable or occasional flaw
    – E.g. @ the native resolution the test fails, multiple Hot-plugs fixes error
  - 8 = fixable or occasional flaw, minor
    – E.g. @ mid-range resolution the test fails, occasional random test fail
  - 10 = pass
    – Perfect image

Sink	Source	Firmwa	Test Name	Cable Length
2408WFP	ATI HD3650	1.07	800x600 @ 60	6ft
2408WFP	ATI HD3650	1.07	800x600 @ 72	6ft
2408WFP	ATI HD3650	1.07	800x600 @ 75	6ft
2408WFP	ATI HD3650	1.07	1024x768 @ 60	6ft
2408WFP	ATI HD3650	1.07	1024x768 @ 70	6ft
2408WFP	ATI HD3650	1.07	1024x768 @ 75	6ft
2408WFP	ATI HD3650	1.07	1280x960 @ 60Hz	6ft
2408WFP	ATI HD3650	1.07	1280x960 @ 75Hz	6ft
2408WFP	ATI HD3650	1.07	1280 x1024 @ 60	6ft
2408WFP	ATI HD3650	1.07	1280 x1024 @ 75	6ft
2408WFP	ATI HD3650	1.07	1360x768 @ 60	6ft
2408WFP	ATI HD3650	1.07	1600x1200 60	6ft
2408WFP	ATI HD3650	1.07	1920x1200 @ 60	6ft
2408WFP	ATI HD3650	1.07	Shutdown	6ft
2408WFP	ATI HD3650	1.07	Restart	6ft
2408WFP	ATI HD3650	1.07	Hibernate	6ft
2408WFP	ATI HD3650	1.07	HPD	6ft
2408WFP	ATI HD3650	1.07	Standby	6ft
2408WFP	ATI HD3650	1.07	Timeout	6ft
2408WFP	ATI HD3650	1.07	Single	6ft
2408WFP	ATI HD3650	1.07	Clone	6ft
2408WFP	ATI HD3650	1.07	Extended	6ft
2408WFP	ATI HD3650	1.07	Resolution Fig of Merit	6ft
2408WFP	ATI HD3650	1.07	Overall Fig of Merit	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	800x600 @ 60	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	800x600 @ 72	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	960x600 @ 60	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	960x600 @ 75	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1024x768 @ 60	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1152x864 @ 60Hz	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1152x864 @ 75Hz	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1280x768 @ 60Hz	6ft
1905FP	Lenovo NVIDIA FX2700	1.07	1280x768 @ 75Hz	6ft

Interop Status

Interoperability

	Good interoperability
Windows (Dell) / NVIDIA GeForce 9400GT	Good Interoperability
Windows (Dell)/NVIDIA Quadro NVS 160M	Good Interoperability
Mac OS X (Apple) / NVIDIA GeForce 9400M	Good Interoperability
Windows (Dell) / Intel GMA4500 chipset	Good Interoperability
Windows (Lenovo) / ATI Radeon HD5750	Good Interoperability
Windows (Lenovo) / NVIDIA Quadro FX 2700M	Good Interoperability
Windows (Dell) / NVIDIA GeForce 9400M	Good Interoperability
Windows (HP) / Intel GMA4500 chipset	Good Interoperability
Windows (Intel Customer Reference Board) / Intel HD Graphics	Good Interoperability

Issue requires attention for root cause analysis in PTN3392	No issues found in this category
Medium severity issue with PTN3392	No issues found in this category
Issue unrelated to PTN3392 This is likely due to the source/sink combination	Some issues found in this category
Minor issue with PTN3392 (User recoverable usually with auto-adjust button on the monitor)	A limited number of issues found in this category

Thank you !